AMENDMENT TO THE CLAIMS

Claim 1 (original): A method of fabricating an integrated device, the method comprising:

forming a transistor of an integrated device;

forming a first protective layer over the transistor; and

forming a micro-electro-mechanical system (MEMS) structure over the first protective layer, the MEMS structure including a movable element that is formed using a deposition process at a temperature of at least about 700°C.

Claim 2 (original): The method of claim 1 wherein the movable element comprises a membrane of a pressure transducer.

Claim 3 (original): The method of claim 1 wherein the movable element comprises a membrane of a capacitive micromachined ultrasonic transducer (CMUT).

Claim 4 (original): The method of claim 1 wherein the integrated device comprises a diffractive light modulator.

Claim 5 (original): The method of claim 1 wherein the integrated device comprises a CMUT.

Claim 6 (original): The method of claim 1 wherein the deposition process comprises low-pressure chemical vapor deposition (LPCVD).

Claim 7 (original): The method of claim 1 further comprising:

suspending the movable element over a bottom electrode.

Claim 8 (original): The method of claim 7 wherein the bottom electrode comprises doped polysilicon.

Claim 9 (original): A method of fabricating an integrated device, the method comprising:

forming a plurality of transistors of an integrated device;

forming a capacitive micromachined ultrasonic transducer (CMUT), the CMUT including a membrane that is formed using a high temperature process, the plurality of transistors and the CMUT being formed on a same substrate; and

forming an interconnect line electrically coupling the CMUT and a transistor in the plurality of transistors.

Claim 10 (original): The method of claim 9 wherein the membrane is suspended over a gap.

Claim 11 (original): The method of claim 9 wherein the high temperature process is performed at a temperature of at least about 700°C.

Claim 12 (original): The method of claim 9 wherein the high temperature process comprises low pressure chemical vapor deposition (LPCVD).

Claim 13 (original): The method of claim 9 wherein the CMUT is formed on a protective layer that is formed over the plurality of transistors.

Claim 14 (original): The method of claim 9 further comprising:
exposing the CMUT by etching at least one layer that is formed over the CMUT.

Claim 15 (original): The method of claim 9 further comprising:
wiring the CMUT using a low temperature process.

Claim 16 (original): The method of claim 15 wherein the low temperature process includes plasma processing.

Claims 17-20 (cancelled)